UNIT –I MOS TRANSISTOR PRINCIPLE

1. Define threshold voltage of a MOSFET.

   The threshold voltage of a MOSFET is usually defined as the gate voltage where an inversion layer forms the interface between the insulating layer (oxide) and the substrate (body) of the transistor.

2. What is enhancement mode FET?

   A type of FET in which there are no charge carriers present in the channel, when the gate voltage is in zero. In these devices, the increasing the gate voltage will increases the current flow from source to drain.

3. What specifications you will consider for selecting a MOSFET?
   1. Breakdown voltages
   2. Forward transconductance
   3. Drain source on resistance (R_{ds})
   4. Switching characteristics
   5. Zero gate voltage drain current (I_{dss})
   6. Input capacitance (C_i)

4. What are the steps performed to achieve lithography friendly design?
   1. Checking the layout confirming the design rules (spacing, trace width, shorts).
   2. Check for the less congested areas and increasing the spacing of the nets.

5. State different types of oxidation.
   1. Dry oxidation
   2. Wet oxidation

6. Give the major advantages of IC.
   1. Size is less
   2. High speed
   3. Less power dissipation.

7. What are different generations of integration circuits?
   1. SSI (Small Scale Integration)
   2. MSI (Medium Scale Integration)
   3. LSI (Large Scale Integration)
   4. VLSI (Very Large Scale Integration).

8. Give the variety of integrated circuits (ICs).
   1. More Specialized Circuits (MSC).
   2. Application Specific Integrated Circuits (ASICs).
   3. Systems on Chips (SOC).

9. What are the various silicon wafer preparations?
   1. Crystal growth and doping
   2. Ingot trimming and grinding
   3. Ingot slicing
   4. Wafer polishing and etching
   5. Wafer cleaning.

10. What are the different terminals in MOS transistors?
    1. Drain
    2. Source
    3. Gate.

11. What is depletion mode operation MOS?

    If the channel is initially doped lightly with p-type impurity a conducting channel exists at zero gate voltage and the device is said to operate in depletion mode.

12. What is enhancement mode operation of MOS?

    If the gate field must induce a channel before current can flow and the gate voltage enhances the channel current and such a device is said to the enhancement mode MOS.

13. State the different types of CMOS processes.
    1. p-well process
    2. n-well process
    3. Silicon on insulator process
    4. Twin tub process.

14. What are the steps involved in twin tub process?
    1. Tub formation
    2. Thin oxide construction
    3. Source and drain implantation
    4. Contact cut definition
    5. Metallization.

15. What is latch up?

    Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between VDD and VSS with disastrous results. Careful control during fabrication is necessary to avoid this problem.

16. What is stick diagram?

    It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

17. What are the uses of stick diagram?
    1. It can be drawn much easier and faster than a complex layout.
    2. These are especially important tools for layout built from large cells.

18. Give the various color coding used in stick diagram.

Green	-	n-diffusion
Red	-	Polysilicon
Blue	-	Metal
Yellow	-	Implant
Black	-	Contact areas.

19. What are the advantages of silicon on insulator (SOI) process?
    1. No latch-up
    2. Due to absence of bulks transistor structures are denser than bulk silicon.

20. State the advantages of CMOS process.

1. Low power dissipation
2. High packing density
3. Bidirectional capability
4. Low input impedance
5. Low delay sensitivity to load.

21. What are short channel devices?

Transistors with channel length less than 3 - 5 microns are termed as short channel devices. With short channel devices the ratio between the lateral and vertical dimensions are reduced.

22. State the different operating regions for an MOS transistor.

1. Cut-off region
2. Non-saturated region
3. Saturated region.

23. Define threshold voltage of CMOS.

The threshold voltage, V_t for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, I_{DS} effectively drops to zero.

24. What is body effect?

The threshold voltage V_T is not a constant with respect to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.

25. What is channel length modulation?

The current between drain and source terminals is constant and independent of the applied voltage over the terminals. The effective length of the conductive channel is actually modulated by the applied voltage V_{DS}, increasing V_{DS} causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

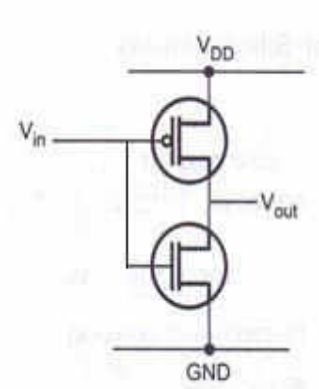
26. Differentiate between channeled and channel less gate array.

S. No.	Channels gate array	Channel less gate array
1.	Only the interconnect is customized.	Only the top few mask layer customized
2.	The interconnect uses predefined cells.	No predefined areas are set aside between spaces between rows of base cells
3.	Routing is done using the spaces	Routing is done using the area of stick unused
4.	Logic density is less	Logic density is higher

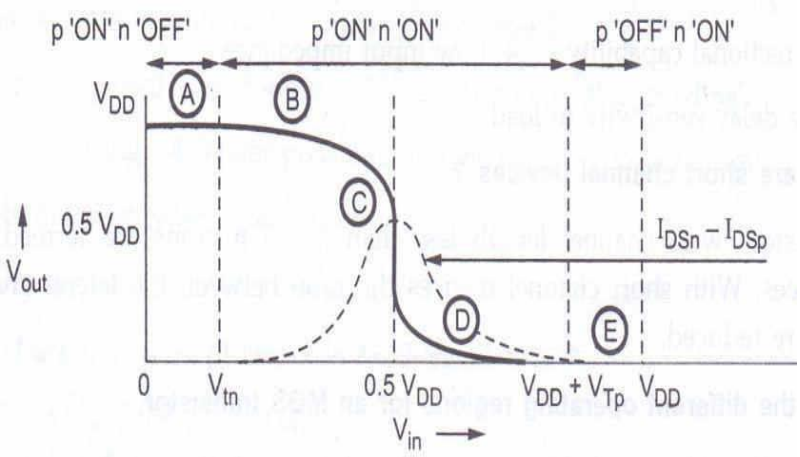
27. Why NMOS technology is preferred than PMOS technology?

N channel transistors have greater switching speed when compared to PMOS transistors.

28. Draw the basic CMOS inverter circuit.



29. Give the CMOS inverter D.C. transfer characteristics and operating regions.



30. Compare PMOS and NMOS

PMOS	NMOS
Current conduction is due to the Holes	Current conduction is due to the electrons
Less switching speed due to lower mobility of holes	Higher switching speed due to greater mobility of electrons
Transistor width is higher	Transistor width is lower
PMOS transistors have greater resistance generally in the range of 2R-3R.	It has lower resistance because of its reduced transistor width.

31. Compare enhancement mode and depletion mode MOSFET.

Enhancement MOSFET	Depletion MOSFET
Device that is normally cut off with zero bias is called as enhancement MOSFET	Device that conducts with zero bias is gate bias called depletion MOSFET
Channel is induced by the gate voltage for current conduction	It has defused channel for current conduction
It operates in enhancement mode only	It operates on enhancement as well as depletion mode.

UNIT II COMBINATIONAL LOGIC CIRCUITS

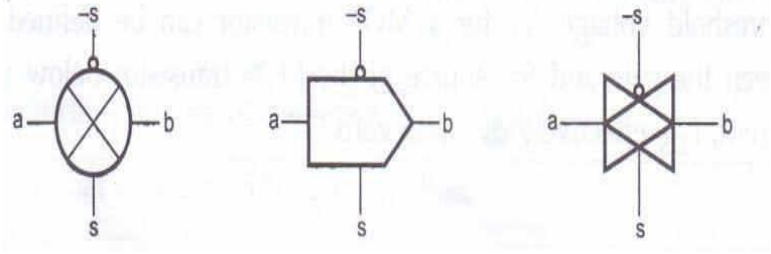
1. What is a pull down device?

   A device connected so as to pull the output voltage to the lower supply voltage usually 0 V is called pull down device.

2. What is pull up device?

   A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

3. Give the different symbols for transmission gate.



4. What is mean by power and power dissipation?

   Power is the rate at which energy is delivered or exchanged; power dissipation is the rate at which energy is taken from the source (VDD) and converted into heat (electrical energy is converted into heat energy during operation).

5. What is mean by PDP?

   Power delay product (PDP) = $P_{av} * t_p = (C_L V_{DD}^2)/2$
   PDP is the average energy consumed per switching event (watts * sec = joule).

6. What is EDP?

   Energy delay product (EDP) = PDP* $t_p = P_{av} * t_p^2$
   EDP is the average energy consumed multiplied by the computation time required.

7. What are two types of power dissipation?

   i) Static dissipation due to leakage current or other current drawn continuously from the power supply.
   ii) Dynamic dissipation due to
      a) Switching transient current.
      b) Charging and discharging of load capacitances.

8. Define elmore delay model.

   It is an analytical method used to estimate the RC delay in a network. Elmore delay model estimates the delay of a RC ladder as the sum over each node in the ladder of the resistance R_{n-1} between that node and a supply multiplied by the capacitor on the nodes.

9. What are the general properties of elmore delay model?
   General property of Elmore delay model network has
   Single input node
   All the capacitors are between a node and ground
   Network does not contain any resistive loop

10. What is static power dissipation?

The power dissipation due to leakage current when the MOS transistor is in idle state is called the static power dissipation. Static power due to

Sub threshold conduction through OFF transistors

Tunneling current through gate oxide

Leakage through reverse biased diodes

Contention current in radioed circuits.

11. What is dynamic power dissipation?

Power dissipation is due to circuit switching to charge and discharge the output load capacitance at a particular node at operating frequency is called dynamic power dissipation.

The Dynamic power dissipation at a particular output node is given by

$P_d=C_L V_{dd}^2 F_{clk} . A$

Where, C_L = Load capacitance

A = Activity factor

V_{dd} = Power supply

F_{clk}= Operating frequency

12. What are the methods available to reduce dynamic power dissipation?

1. Reducing the product of capacitance and its switching frequency.
2. Eliminate logic switching that is not necessary for computation.
3. Reduce activity factor Reduce supply voltage

13. What are the methods to reduce static power dissipation?

1. By selecting multi threshold voltages on circuit paths with low-V_t transistors while leakage on other paths with high-V_t transistors.
2. By using two operating modes, active and standby for each function blocks.
3. By adjusting the body bias (i.e) adjusting FBB (Forward Body Bias) in active mode to increase performance and RBB (Reverse Body Bias) in standby mode to reduce leakage.
4. By using sleep transistors to isolate the supply from the block to achieve significant leakage power savings.

14. What is short circuit power dissipation?

During switching, both NMOS and PMOS transistors will conduct simultaneously and provide a direct path between VDD to ground resulting in short circuit power dissipation.

15. Define design margin.

The additional performance capability above required standard basic system parameters that may be specified by a system designer to compensate for uncertainties is called design margin. Design margin required as there are three sources of variation two environmental and one manufacturing.

16. Write the applications of transmission gate?

Multiplexing element of path selector

A latch element an unlock switch

Act as a voltage controlled resistor connecting the input and output.

17. What is pass transistor?

It is a MOS transistor, in which gate is driven by a control signal, when the control signal is high, input is passed to the output and when the control signal is low, the output is floating topology such topology circuits is called pass transistor.

18. List the advantages of pass transistor logic.

Pass transistor logic circuits are often superior to standard CMOS circuits in terms of layout density, circuit delay and power consumption.

They do not have path VDD to GND and do not dissipate standby power (static power dissipation).

19. What is transmission gate?

The circuit constructed with the parallel connection of PMOS and NMOS with shorted drain and source terminals. The gate terminal uses two select signals s and , when s is high than the transmission gate passes the signal on the input. The main advantage of transmission gate is that it eliminates the threshold voltage drop.

20. Why low power has become an important issue in the VLSI circuit realization? Increasing transistor count:

The number of transistor is getting doubled in every 18 months based on moore's law Higher speed of operation:

The power dissipation is proportional to clock frequency Greater device leakage current:

In nanometer technology the leakage component become a significant percentage of the total power and the leakage current increases at a faster rate than dynamic power in technology generations.

21. What are the various ways to reduce the delay time of a CMOS inverter?

1. The width of the MOS transistor can be increased to reduce delay this is known as gate sizing, which will be discussed later in more details.
2. The load capacitance can be reduced to reduce delay this is achieved by using transistor of smaller and smaller dimension by feature generation technology.
3. Delay can also be reduced by increasing the supply voltage VDD and reducing the threshold voltage V_t of the MOS transistors

22. Explain the basic operation of a 2- phase dynamic circuit.

The operation of the circuit can be explained using pre-charge logic in which the output is pre-charged to HIGH level during Φ_2 clock and the output is evaluated during Φ_1 clock.

23. What makes dynamic CMOS circuits faster than static CMOS circuits?

As MOS dynamic circuits require lesser number of transistors and capacitance is to be driven by it. This makes MOS dynamic circuits faster.

24. What is glitch power dissipation?

Because of finite delay of the gates used to realize the Boolean functions, different signals cannot reach the inputs of a gate simultaneously this leads to spurious transition at the output before it settles down to its final value, the spurious transitions leads to charging and discharging of the outputs causing glitch power dissipation.

UNIT III SEQUENTIAL LOGIC CIRCUITS

1. What is metastability and list the steps to prevent it?

Metastability is an unknown state it is neither zero nor one. Metastability happens for the design systems violating setup or hold time requirements. Setup time is a requirement that the data has to be stable before the clock edge and hold time is a requirement that the data has to be stable after the clock edge. The potential violation of the setup and hold violation can happen when the data is purely asynchronous and clocked synchronously. Steps to prevent metastability:

1. Using proper synchronizers (two stage or three stage), as soon as the data is coming from the asynchronous domain. Using synchronizers, recovers from the metastable event.
2. Use synchronizers between cross-clocking domains to reduce the possibility from metastability.
3. Using faster flip flops (which has narrower metastable window).

2. Define local-skew, global-skew, and useful-skew. Local skew:

The difference between the clock reaching at the launching flip-flop vs the clock reaching the destination flip-flop of a timing-path.

Global skew:

The difference between the earliest reaching flip-flop and latest reaching flip-flop for a same clock-domain.

Useful skew:

Useful skew is a concept of delaying the capturing flip-flop clock path, this approach helps in meeting setup requirement within the launch and capture timing path. But the hold requirement has to be met for the design.

3. What is meant by virtual clock definition and why it is needed?

Virtual clock is mainly used to model the I/O timing specification. Based on what clock the output/input pads are passing the data.

4. What is the difference between mealy and moore state machines?

In the mealy state machine we can calculate the next state and output both from the input and state. But in the moore state machine we can calculate only next state but not output from the input and state and the output is issued according to next state.

5. What is the difference between latches and flip-flops based designs?

Latches are level-sensitive and flip-flops are edge sensitive. Latch based design and flop based design is that latch allows time borrowing which a tradition flip-flop does not: That makes latch based design more efficient. But at the same time, latch based design is more complicated and has more issues in min timing (races).

6. What are the classifications of CMOS circuit families? Static CMOS circuits.

Dynamic CMOS circuits.
Ratioed circuits. Pass-transistor circuits.

7. What are the characteristics of Static CMOS design?

A static CMOS circuit is a combination of two networks, one is pull-up network (PUN) and the other is pull-down network (PDN) in which at every point in time, each gate output is connected to either VDD or VSS via pull-up or pull down network.

8. List the important properties of Static CMOS design.
    1. At any instant of time, the output of the gate is directly connected to VDD and VSS.
    2. The function of the PUN is providing a connection between the output and VDD.
    3. The function of the PDN is providing a connection between the output and VSS.
    4. Both PDN and PUN are constructed in mutually exclusive way such that one and only one of the networks is conduct in steady state. That is, the output node is always a low-impedance node in steady state.

9. What is Dynamic CMOS logic?

Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance node. It requires only N+2 transistors. It takes a sequence of precharge and conditional evaluation phases to realize the logic functions.

10. What are the properties of dynamic logic?
    1. Logic function is implemented by pull-down network only.
    2. Full swing outputs (V_{OL}= GND and V_{OH} = VDD).
    3. Non-ratioed.
    4. Faster switching speeds.
    5. Needs a precharge clock.

11. What are the disadvantages of dynamic CMOS technology?

A fundamental difficulty with dynamic circuits is a loss of noise immunity and a serious timing restriction on the inputs of the gate. Violate monotonicity during evaluation phase.

12. What is CMOS Domino logic?

A static CMOS inverter placed between dynamic gates which eliminate the monotonicity problem in dynamic circuits are called CMOS Domino logic.

13. What is called static and dynamic sequencing element?

A sequencing element with static storage employs some sort of feedback to retain its output value indefinitely. A sequencing element with dynamic storage generally maintains its value as charge on a capacitor that will leak away if not refreshed for a long period of time.

14. What is clock skew?

In reality clocks have some uncertainty in their arrival times that can cut into the time available for useful computation. It is called clock skew.

15. What are synchronizers?

Synchronizers are used to reduce metastability. The synchronizers ensure synchronization between asynchronous input and synchronous system.

16. Difference between latches and Flip-Flop.

S.No	Latch	Flip-Flop
1.	A Latch is Level Sensitive	A flip-flop is edge triggered.
2.	A latch stores when the clock level is low and is transparent when the level is high.	A flip-flop stores when the clock rises and is mostly never transparent.

17. Define Pipelining.

Pipelining is a popular design technique often used to accelerate the operation of the data path in digital processors. The major advantages of pipelining are to reduce glitch in complex logic networks and getting lower energy due to operand isolation.

18. How the limitations of a ROM based realization is overcome in a PLA based realization. In a ROM, the encoder part is only programmable and use of ROMs to realize

Boolean functions is wasteful in many situations because there is no cross-connect for a significant part. This wastage can be overcome by using Programmable Logic Array (PLA), which requires much lesser chip area.

19. Define Latch/flip-flop clock-to-Q propagation delay.

t_{PLH}: 50% triggering edge point of the clock pulse to 50% transition of the output from low to high.

t_{PHL}: 50% triggering edge of the clock pulse to the high to low transition of the output.

20. Define Latch/flip-flop clock-to-Q contamination delay.

Output signal start to change after its input change and settles to the final value within propagation delay.

21. What is static 0 hazard?

Output goes momentarily 1 when it should remain at 0 is called static 0 hazard.

22. What is dynamic hazard?

Output changes 3 or more times when it changes from 1 to 0 or 0 to 1

23. What is non critical race?

Final stable state does not depend on the order in which the state variable changes then that race is called non critical race and it is not harmful

24. What is critical race?

Final stable state depends on the order in which the state variable changes then that race condition is called critical race and it is harmful.

25. Define propagation delay and contamination delay?

Propagation delay: The amount of time needed for a change in a logic input to result in a permanent change at an output that is the combinational logic will not show any further output changes in response to an input change.

Contamination delay: The amount of time needed for a change in a logic input to result in an initial change at an output, that is the combinational logic is guaranteed not to show any output change in response to an input change before fed time units have passed.

26. Define Setup time and Hold time.

Setup time (t_{setup}): The amount of time before the clock edge that data input D must be stable the rising clock edge arrives.

Hold time (t_{hold}): This indicates the amount of time after the clock edge, the data input D must be held stable in order for Flip Flop to latch the correct value. Hold time is always measured from the rising clock edge to a point after the clock edge.

27. Differentiate DRAMs from SRAMs.

Both SRAMs and DRAMs are volatile in nature, ie. Information is lost if power line is removed. However SRAMs provide high switching speed, good noise margin but require large chip area than DRAMs.

28. Explain the read and write operations for a one transistor DRAM cell.

A significant improvement in the DRAM evolution was to realize 1-T DRAM cell. One additional capacitor is explicitly fabricated for storage purpose. To store '1', it is charged and to store '0' it is discharged to '0' volt. Read operation is destructive. Sense amplifier is needed for reading. Read operation is followed by restoration operation.

UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS

1. How data path can be implemented in VLSI system?

A data path is best implemented in a bit-sliced fashion. A single layout is used repetitively for every bit in the data word. This regular approach eases the design effort and results in fast and dense layouts

2. Write short note on the performance of ripple carry adder.

A ripple carry adder has a performance that is linearly proportional to the number of bits. Circuit optimizations concentrate on reducing the delay of the carry path. A number of circuit topologies exist proving that careful optimization of the circuit topology and the transistor sizes helps to reduce the capacitance on the carry bit

3. What are the advantages of ripple carry adder? Circuit realization is very simple
Consumes less power
Compact layout giving smaller chip area

4. What is carry skip adder?

A carry skip adder consists of a simple ripple carry adder with a special speed up carry chain called a skip chain. The carry skip circuitry consists of two logic gates. The AND gate accepts the carry in bit and compares it to the group propagate signal.

5. What is mirror adder?

In this circuit realization the PMOS network is identical to the NMOS network rather than being the conduction complement, so the topology is called a mirror adder.

6. What are the advantages of carry skip adder?

The propagation delay is smaller compare to ripple carry adder when optimal stages are used.

The carry skip adder is shown to be superior to constant width carry skip module the advantages being greater at high precisions.

7. What is the logic of adder for increasing its performance?

Other adder structures use logic optimizations to increase the performance (carry-bypass, carry select, carry look ahead). Performance increase comes at the cost of area.

8. What is a multiplier circuit?

A multiplier is nothing more than a collection of cascaded adders. Critical path is far more complex and optimizations are different compared to adders.

9. Define input ordering.

For PMOS and NMOS the inner inputs encounters the body effect and requires high threshold voltage to turn on. By input ordering the rare changing inputs are moved to inner inputs. This provides sufficient power saving.

10. Which factors dominates the performance of a programmable shifter?

The performance and the area of a programmable shifter are dominated by the wiring.

11. Write down the expression for worst case delay for
RCA. $t = (n-1)\ t_c + t_s$

12. Write down the expression to obtain delay for N-bit carry bypass adder.
$t_{adder} = t_{setup} + M*t_{carry} + (N/M-1)*t_{bypass} + (M-1)*t_{carry} + t_{sum}$

13. Define braun multiplier.

The simplest multiplier is the Braun multiplier. All the partial products are computed in parallel, and then collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. This multiplier is suitable for positive operands.

14. Why we go for booth's algorithm?

Booth algorithm is a method that will reduce the number of multiplicand multiples. For a given number of ranges to be represented, a higher representation radix leads to fewer digits.

15. List the different types of
shifter. Array shifter
Barrel shifter
Logarithm shifter

16. What are the various shift operations
available? Logical left shift
Logical right shift
Arithmetic left shift
Arithmetic right shift

17. What is the output after two arithmetic right shift for A=1001?

Input	= 1001
After first arithmetic right shift	= 1100
After second arithmetic right shift	= 1110

18. What is a Manjestor carry chain adder?

It uses a cascade of pass transistors to implement the carry chain. Propogate & generate signals are generated using pass transistor logic. The capacitance per node on the carry chain is very small & equals only 4 diffusion capacitances.

19. Why is carry bypass Adder called so?

When the bypass control signal is set to '1', the incoming carry is forwarded immediately to the next block through a bypass transistor.

20. What is the importance of linear carry select Adder?

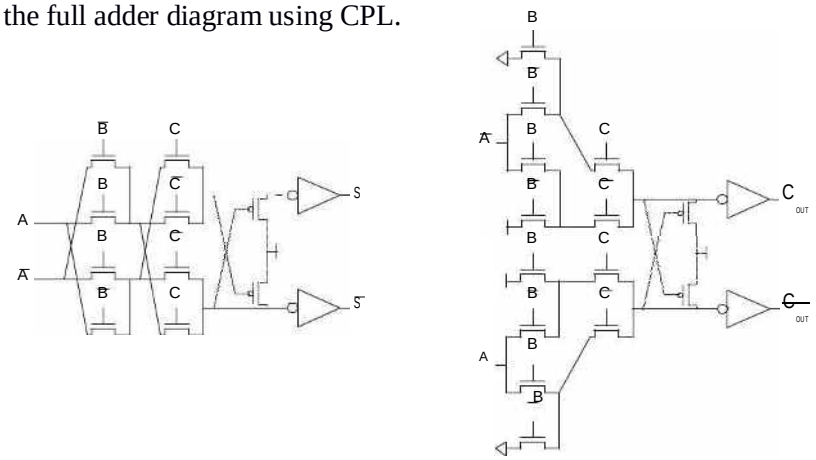
The linear dependencies present in a ripple carry adder is avoided in linear carry select adder, by anticipating both possible values of the carry i/p and evaluate the result for both possibilities in advance.

21. Why is the propagation delay in a carry select Adder is linearly proportional to N? It is because the block select signal that selects between 0&1 solutions still has to ripple through all stages in worst case.

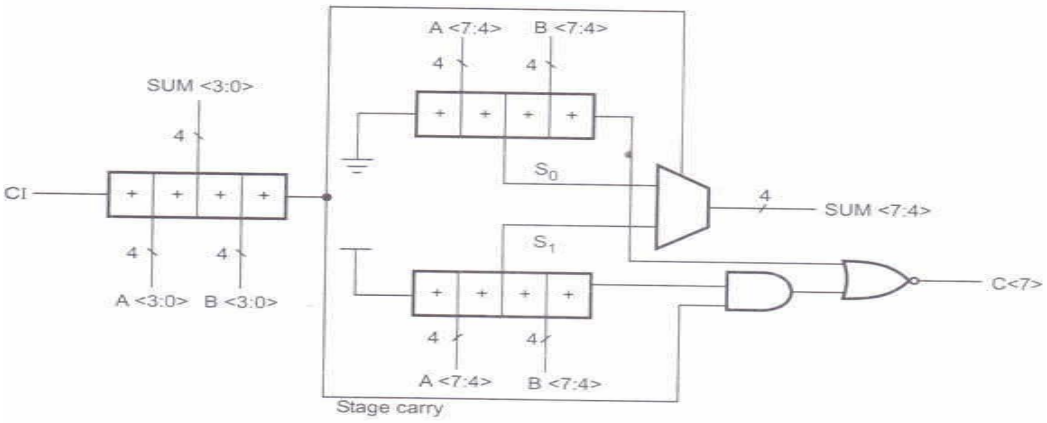
22. What is a bit serial multiplier?

When area is of prime concern, it is possible to reduce the cost of the multiplier by using a time multiplexed approach .Here, a combination of a single adder & a storage element is used to iteratively compute the summation of the partial products.

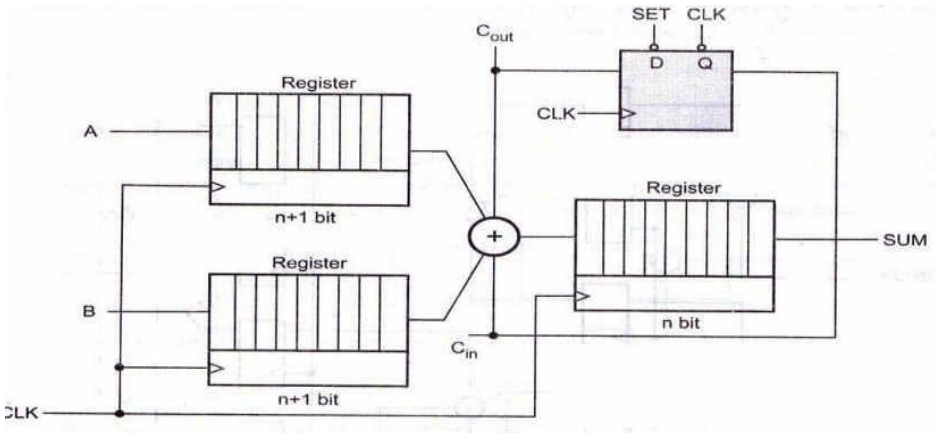
23. Draw the full adder diagram using CPL.



24. Draw the block diagram carr y select adder.



25. Draw the block diagram of se rial adder.



UNIT V IMPLEMENTATION STRATEGIES

1. What is the standard cell based ASIC design?

A cell based ASIC (CHIC) uses predesigned logic cells known as standard cells. The standard cell areas also called flexible blocks in a CHIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and interconnection in a CHIC. All the mask layers of a CHIC are customized and are unique to a particular customer.

2. What is a FPGA?

A Field Programmable Gate Array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of up to about 20,000 equivalent gates.

3. What are the different methods of programming of PALS?
   1) Fusible links
   2) UV - Erasable EPROM
   3) EEPROM (E^2PROM) - Electrically Erasable Programmable ROM.

4. What is an antifuse?

An antifuse is normally high resistance (>100 MW). On application of appropriate programming voltages, the antifuse is changed permanently to a low resistance structure (200-500 W).

5. Differentiate between channeled and channel less gate array.

Channeled gate array	Channel less gate array
Only the interconnect is customized	Only the top few mask layers are customized
The interconnect uses predefined spaces between rows of base cells	No predefined areas are set aside for routing between cells.
Routing is done using spaces	Routing is done using the area of transistors unused
Logic density is less	Logic density is higher

6. What are the different levels of design abstraction at physical design? Architectural or functional unit
   Register Transfer level
   (RTL) Logic level
   Circuit level

7. What are macros?
   The logic cells in a gate array are often called as macros.

8. What are programmable Interconnects?

In a PAL, the device is programmed by changing the characteristics if the switching element. An alternative would be to program the routing.

9. What are the types of ASICs?
   Full custom ASICs Semi
   custom ASICs

10. What are the types of programmable
    devices? Programmable logic structure
    Programmable Interconnect
    Reprogrammable Gate Array

11. What are the features of standard celled ASICs?
    All mask layers are customized-transistors and interconnect.
    Custom blocks can be embedded
    Manufacturing lead time is about eight weeks.

12. What are the characteristics of FPGA? None
    of the mask layers are customized
    A method of programming the basic logic cells and the interconnect.
    The core is a array of programmable basic logic cells that can
    implement combinational as well as sequential logic (flip flops).
    A matrix of programmable interconnect surrounds the basic logic
    cells. Design turnaround is a few hours.

13. What is programmable logic array?

    A programmable logic array (PLA) is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a programmable OR planes, which can then be conditionally complemented to produce an output. This layout allows for a large number of logic functions to be synthesized in the sum of products canonical forms.

14. What is meant by programmable logic plane?

    The programmable logic plane is programmable read only memory (PROM) array that allows the signals present on the devices pins to be routed to an output logic macro cell.

15. Define ROM

    A read only memory (ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each bit combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2n.

16. What is the full custom ASIC design?

    In a Full custom ASIC, an engineer designs some or all of the logic cells, circuits and layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

17. Why was PAL developed?

    It was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

18. State the types of ROM
    Masked ROM.
    Programmable Read only Memory Erasable Programmable Read only memory.
    Electrically Erasable Programmable Read only Memory.

19. List the major differences between PLA and PAL PLA
    Both AND and OR arrays are programmable and Complex Costlier than PAL
    PAL
    AND arrays are programmable OR arrays are fixed Cheaper and Simpler

20. Give the different types of ASIC.
    1. Full custom ASICs
    2. Semicustom ASICs

    3. Programmable ASICs Programmable Logic Device (PLD) Field Programmable Gate Array (FPGA).